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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,050	03/18/2004	Iain Christopher Butler	SONY-27800	7987

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EXAMINER	
CHOE, HENRY	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,050	BUTLER, IAIN CHRISTOPHER	
	Examiner	Art Unit	
	Henry K. Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-24* is/are allowed.

6)☒ Claim(s) *1,2,7,13,14,28-30,35,36,40-42,47 and 48* is/are rejected.

7)☒ Claim(s) *3-6,8-12,26,27,31-34,38,39 and 43-46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7, 13, 14, 25, 28-30, 35-37, 40-42, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al (Fig. 2) in view of Chambers (Fig. 4).

Regarding claim 1, Yamamoto et al (Fig. 2) discloses an amplifier circuit comprising the transistors (M1-M4, Vc, CM1, CM2) which can be read as the claimed grounded source operational amplifier circuit since the sources of transistors M1-M4 are directly coupled to the ground (GND). However, Yamamoto et al (Fig. 2) does not disclose a dynamic current switching circuit. Chambers (Fig. 4) discloses an amplifier circuit comprising an operational transconductance amplifier (400) which can be read as the claimed dynamic current switching circuit since the operational transconductance amplifier (400) provides reduced static current dissipation and improved dynamic performance (see column 10, lines 61-64). It would have been obvious to one of ordinary skill in the art, at the time the invention was made would have found it obvious to have employed the dynamic current switching circuit at the outputs of the grounded source operational amplifier circuit of Yamamoto et al (Fig. 2), such as taught by Chambers (Fig. 4) in order to provide the advantageous benefit of reducing power dissipation (see column 1, lines 42-43).

Regarding claim 2, the grounded source operational amplifier circuit (M1-M4, Vc, CM1, CM2) of Yamamoto et al (Fig. 2) includes a main amplifier core circuit (M1-M4) and the current mirrors (CM1, CM2) which can be read as the claimed biasing circuit since the current mirrors (CM1, CM2) affect the bias voltages of the main amplifier core circuit (M1-M4).

Regarding claims 7, 30 and 42, the dynamic current switching circuit (400) of Chambers (Fig. 4) includes a main mirror diode (496), a main fixed current source (468), a first current switch (484), and a second current switch (486).

Regarding claims 25 and 37, Yamamoto et al (Fig. 2) discloses an amplifier circuit comprising a main amplifier core circuit (M1-M4) including a first main leg (a connection between a drain of transistor M1 and CM1) and a second main leg (a

connection between a drain of transistor M2 and CM2), current mirrors (CM1, CM2) which can be read as the claimed biasing circuit since the current mirrors (CM1, CM2) affect the bias voltages of the main amplifier core circuit (M1-M4). However, Yamamoto et al (Fig. 2) does not disclose a dynamic current switching circuit. Chambers (Fig. 4) discloses an amplifier circuit comprising an operational transconductance amplifier (400) which can be read as the claimed dynamic current switching circuit since the operational transconductance amplifier (400) provides reduced static current dissipation and improved dynamic performance (see column 10, lines 61-64). It would have been obvious to one of ordinary skill in the art, at the time the invention was made would have found it obvious to have employed the dynamic current switching circuit at the outputs of the main amplifier core circuit of Yamamoto et al (Fig. 2), such as taught by Chambers (Fig. 4) in order to provide the advantageous benefit of reducing power dissipation (see column 1, lines 42-43).

Regarding claims 13, 14, 28, 29, 35, 36, 40, 41, 47 and 48, the combination of Yamamoto et al (Fig. 2) and Chambers (Fig. 4) discloses all the limitations in the claims except for that the common mode output voltage is about 1.5V, common mode input voltage is about 1.1V, upper gain bias voltage is about 500mV, and lower gain bias voltage is about 400mV. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the specific values of the common mode output and input voltages, and upper and lower gain bias voltages, since they are based on the routine experimentation to obtain the optimum operating parameters.

Allowable Subject Matter

Claims 3-6, 8-12, 26, 27, 31-34, 38, 39 and 43-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

Claims 15-24 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 15, the closest prior art of record, Yamamoto et al (Fig. 2) does not disclose at least the following limitations: the physical structures of the upper and lower gain enhancement circuits.

Response to Arguments

Applicant's arguments with respect to claims 1-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,724,258; 6,624,698) are the grounded source operational amplifier circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER